UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,933	03/23/2001	Christian Siemers	GR 98 P 8110 P	6157

24131 7590 03/18/2004

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
SIDDIQI, MOHAMMAD A	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 03/18/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

3

Office Action Summary	Application No.	Applicant(s)	
	09/816,933	SIEMERS, CHRISTIAN	
	Examiner	Art Unit	
	Mohammad A Siddiqi	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) *39-76* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-76 are presented for examination. Claims 39-76 are withdrawn from examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Kau et al. (6421754) (hereinafter Kau).

4. As per claims 1 and 20, Kau discloses a program-controlled unit (see abstract), comprising: an intelligent core configured (figure 9, element 702,701) to process instructions to be executed (figure 19, col 123, lines 29-67);

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit (figure 9, element 718,702,726), external peripheral units exterior to the program-controlled unit (figure 3, element IN6, and IN7, col 9, lines 1-64), and one or more memory devices (figure 3, element 74, IN6, and IN7, col 9, lines 1-64);

a structurable hardware unit (figure 3, col 9, lines 1-64) selectively forming an application-specifically (figure 45, element 4350, col 49, lines 28-47) configurable intelligent interface for respectively connecting said intelligent core (figure 9, element 702) and said units (figure 9, col 49, lines 28-47), including an interface connection between said intelligent core and said internal peripheral units (figure 3, col 61, lines1-11), between said intelligent core and said external peripheral units(figure 67,col 61, lines 15-26), , between said intelligent core and said memory devices(figure 3, element 702, 718), and between said plurality of units(figure 9); and

wherein said structurable hardware unit (figure 3) is configured to evaluate and process data (figure 9) and/or signals (col 63, lines66-67) received thereby (fig 9, Col 64, lines 1-8).

5. As per claims 2 and 21, Kau discloses the structurable hardware (figure 3) unit is disposed in circuit (col 2, lines 14-42) terms between said intelligent core (figure 9, element 702) and said plurality of units (col 2, lines 14-42).

6. As per claims 3 and 22, Kau discloses the structurable hardware unit (figure 3) is connected to a multiplicity of potential data (figure 61, element 302, lines 14-36) and signal sources and data and signal destinations (col 48, lines 51-53), and wherein a plurality of multiplexers (figure 61, element 6110, 6120, col 60, lines 14-36) are connected to said structurable hardware unit (figure 3) for selecting current data and signal sources and current data and signal destinations (figure 61, element 6110, 6120, col 60, lines 14-36).

7. As per claims 4 and 23, Kau discloses the data and signal sources (col 48, lines 37-53) and the data and signal destinations comprise (col 48, lines 51-53) units selected from the group of units consisting of said intelligent core (figure 9, element 702), said peripheral units (figure 3), said memory devices (figure 3, element 74, IN6, and IN7, col 9, lines 1-64), and portions of said structurable hardware unit (figure 3, element 74, IN6, and IN7, col 9, lines 1-64).

8. As per claims 5 and 24, Kau discloses a structuring of said structurable hardware (figure 3) unit selectively results in an alteration of given data paths and in a configuration of logic elements (col 43, lines 19-27).

9. As per claims 6 and 25, Kau discloses a structurable hardware unit (figure 3) comprises a clock generation unit generating a clock signal (figure 27, element 2510, col 37, lines 52-57) and a logic block unit connected to receive the clock signal (figure 27, col 34, lines 52-67), said logic block unit enabling devices to be connected via said structurable hardware unit to cooperate as desired (col 35, lines 1-46).

10. As per claims 7 and 26, Kau discloses the clock generation unit and said logic block unit each contain configurable elements (figure 27, element 2510, col 37, lines 52-67).

11. As per claims 8 and 27, Kau discloses the clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration (col 35, lines 55), a NAND array (col 32, lines 112), a multiplexer-based logic variant (figure 61, element 6110, 6120, col 60, lines 14-36), and a structurable logic configuration (col 89, lines 47-54).

12. As per claims 9 and 28, Kau discloses the logic block unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array (figure 27, col 35, lines 62-67 and col 36, lines 1-50), a multiplexer-based logic variant, and a structurable logic configuration (figure 61, element 6110, 6120, col 60, lines 14-36).

13. As per claims 10 and 29, Kau discloses the logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks (col 123, lines 1-67).

14. As per claims 11 and 30, Kau discloses one of sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block (col 67 and 68, table).

15. As per claims 12 and 31, Kau discloses one of sub-blocks is configured as a state machine for central sequence control (figure 22, element 2030, lines 15 –42).

16. As per claims 13 and 32, Kau discloses one of sub-blocks is configured as an address calculation device for calculating source and destination addresses (col 67,68, 69,and 70).

17. As per claims 14 and 33, Kau discloses one of sub-blocks is configured as an instruction injection device for injecting instructions into an instruction pipeline of said intelligent core (col 66, lines 55-60).

18. As per claims 15 and 34, Kau discloses the structurable hardware unit (figure 3) is configurable with devices selected from the group consisting of fuses and anti-fuses (col 14, lines 58-67).

19. As per claims 16 and 35, Kau discloses the structurable hardware unit (figure 3) is reversibly configurable (col 143, lines 14-19).

20. As per claims 17 and 36, Kau discloses the structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core (figure 57, col 182, lines 57-65).

21. As per claims 18 and 37, Kau discloses a configuration of structurable hardware unit (figure 3) is enabled only at predetermined times (col 151, lines 1-5).

22. As per claims 19 and 38, Kau discloses the program-controlled configuration of structurable hardware unit (figure 3) is enabled at any time (col 128, lines 39-41).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Response to Arguments

23. Applicant's arguments filed 02/02/04 have been fully considered but they are not persuasive:

In response to applicant's argument " Kau et al. do not show a structurable hardware unit", the examiner respectfully disagrees. The Kau prior art reference teaches structurable hardware unit (fig 3) intelligent interface for respectively connecting (col 9, lines 38 –45) an intelligent core and the units (fig 9, element 702, col 10, lines 56-67). Therefore, limitations are met by the reference. Claims 1 stand rejected.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad A Siddiqi whose telephone number is (703) 305-0353. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703) 305-

8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAS

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100